REMARKS

Claims 1-13 remain present in this application.

The specification and claims 1 and 8 have been amended. Reconsideration of the application, as amended, is respectfully requested.

Rejection under 35 USC 112

Claims 1 and 8 stand rejected under 35 USC 112, second paragraph. This rejection is respectfully traversed.

In view of the foregoing amendments, in which the Examiner's helpful instructions have been followed, it is respectfully submitted that all claims particularly point out and distinctly claim the subject matter of the instant invention. Accordingly, reconsideration and withdrawal of the 35 USC 112, second paragraph rejection are respectfully requested.

Rejections under 35 USC 103

Claims 1-13 stand rejected under 35 USC 103 as being unpatentable over the Applicant's Admitted Prior Art (AAPA) in view of Meynard, US Publication 2003/0229816. This rejection is respectfully traversed.

Claims 3 and 5 stand rejected under 35 USC 103 as being unpatentable over the Applicant's Admitted Prior Art in view of Meynard, and further in view of Cheng et al., U.S. Patent 6,963,992. This rejection is respectfully traversed.

The Examiner is reminded that, in order to establish a prima facie case of obviousness, three criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teaching. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See MPEP 2142.

With respect to independent claims 1 and 8, these claims recite (emphasis added):

> 1. A power voltage control circuit for a CPU, wherein the CPU has at least one power indication pin to output a power indication signal, the control circuit comprising:
>
> a selection unit having a first input terminal coupled to the power indication pin, a second input terminal and a control terminal;
>
> a register to store an adjustment signal;
>
> ***a combination unit to produce a first signal and output to the second terminal of the selection unit according to the power indication signal and the adjustment signal***;
>
> a selection controller to output a selection signal to the control terminal of the selection unit, such that the selection unit outputting one power indication signal or the first signal; and
>
> a PWM controller coupled to the selection unit to produce a power voltage to the CPU according to the power indication signal or the first signal.
>
> 8. A control circuit for power voltage of a CPU, wherein the CPU has at least one power indication pin to output a power indication signal, and the CPU adjusts the power indication signal according to load and operating temperature thereof, the control circuit comprising:
>
> a selection unit having a first input terminal coupled to the power indication pin, a second input terminal and a control terminal;
>
> ***a combination unit to produce a first signal and output to the second terminal of the selection unit according to the power indication signal and an adjustment signal***;
>
> a selection controller to output a selection signal to the control terminal of the selection unit, such that the selection unit outputting one power indication signal or the first signal; and
>
> a PWM controller coupled to the selection unit to supply a power voltage to the CPU according to the power indication signal or the first signal.

Turning now to the Applicant's Admitted Prior Art, the Applicant's Admitted Prior Art sets forth that the control circuit cannot adjust the power voltage to the CPU 10, as CPU load and operating temperature fluctuate when the control signal S_{VID} from the CPU is isolated from the PWM controller 12 by MUX 20 due to the selection signal Sel (during overclock mode). Thus, the control circuit cannot efficiently provide the correct voltage necessary to overclock the CPU 10 (see page 2 and Fig. 2). Namely, the Applicant's Admitted Prior Art does not disclose a combination unit 140 producing a first signal S1 to output to the second terminal of the selection unit 130 according to the power indication signal S_{VID} and an adjustment signal Sa (during overclock mode).

Turning now to Meynard, this publication discloses a clock control arrangement for a computer system which includes chipset 220 which communicates with the processor 210 with GTL bus 290 with a set control set for monitoring the activity of the processor 210, a control unit 230 which performs an analysis of the activity of the processor, a temperature sensing device 280 which transmits information representative of the temperature of the chip, and a controllable clock circuit 270 which produces the clock required for driving processor 210. The clock circuit 270 produces at least two different clock signals, a first one with one given frequency (F1) and a second one of a higher frequency (F2). In the case of overclocking, the BNR control signal is used for controlling the clock circuit 270, so that the latter produces the higher frequency value to the processor 210, increasing the performance of the computer system (see paragraphs [0050]-[0057]). Namely, in order to overclock or downclock, Meynard teaches only adjustment of clock frequency rather than power voltage, as asserted by the Examiner.

Further, as discussed in paragraph [0013], Meynard discloses that the clock control arrangement is carried out independently of the operating system which is running within the computer system, and also ***independently of the power management functions which operate in the system***. Namely, Meynard teaches that the clock control arrangement should not be executed with power voltage adjustment. Thus, Meynard teaches away from the claimed invention.

The secondary reference to Cheng et al. fails to overcome the deficiencies of the primary references.

Under MPEP2143, in order to establish a prima facie case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. In particular, as set fourth above, applicant respectfully asserts that neither Meynard nor the Applicant's Admitted Prior Art teaches or reasonably suggests all of the limitations found in independent claims 1 and 8. It is therefore respectfully submitted that the control circuit of independent claims 1 and 8 is neither taught nor suggested by the prior art utilized by the Examiner. Accordingly, reconsideration and withdrawal of the 35 USC 103 rejections are respectfully requested.

Conclusion

Favorable reconsideration and an early Notice of Allowance are earnestly solicited.

Because the additional prior art cited by the Examiner has been included merely to show the state of the prior art and has not been utilized to reject the claims, no further comments concerning these documents are considered necessary at this time.

In the event that any outstanding matters remain in this application, the Examiner is invited to contact the undersigned at (703) 205-8000 in the Washington, D.C. area.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2448 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17; particularly, extension of time fees.

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Respectfully submitted,

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